Notice of Allowability	Application No.	Applicant(s)	
	10/709,641	TSENG ET AL.	
	Examiner	Art Unit	
	Yong Sim	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/20/07*.

2. ☒ The allowed claim(s) is/are *1 and 3 - 24*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given by Belinda Lee on 7/20/07.

The application has been amended as follows:

Claim 1. (currently amended) A source driver for driving sources of a plurality of thin film transistors, the source driver comprising:

a shift register, for receiving digital image data;

a latch, coupled to the shift register, for receiving digital image data from the shift register;

a first level shifter with a positive polarity and a second level shift with a negative polarity [[a plurality of level shifters]], coupled to the latch, for receiving digital image data from the latch and for shifting a voltage level of digital image data; and

a first analog circuit with a positive polarity and a second analog circuit with a negative polarity [[a plurality of analog circuits]], coupled to the first level shifter with the positive polarity and the second level shifter with the negative polarity respectively [[the level shifter]], for receiving the digital image data, converting the digital image data to a corresponding analog image data, and outputting the analog image data to the plurality

of sources of the thin film transistors;

wherein a power supply voltage level and a middle voltage level between the power supply voltage level and a ground voltage level are provided to the first level shifter with the positive polarity and the first analog circuit with the positive polarity; and the middle voltage level and the ground voltage level are provided to the second level shifter with the negative polarity and the second analog circuit with the negative polarity. ~~a power supply voltage level and a ground voltage level are provided to the level shifter and the analog circuit; at least one middle voltage level between the power supply voltage level and the ground voltage level is provided to the level shifters and the analog circuits, each of the level shifters and the analog circuits has a positive polarity or a negative polarity; the a power supply voltage level and the middle voltage level are provided to the level shifter with the positive polarity and the analog circuit with the positive polarity; and the middle voltage level and the ground level are provided to the level shifter with the negative polarity and the analog circuit with the negative polarity.~~

Claim 3. (currently amended) The source driver of claim 1, wherein when there are two or more middle voltage levels are provided, the middle voltage level provided to the first level shifter with the positive polarity and the first analog circuit with the positive polarity is larger than the ground voltage level and equal to or less than a half of the power supply voltage level, and the middle voltage level provided to the second level shifter with the negative polarity and the second analog circuit with the negative polarity

is larger than or equal to a half of the power supply voltage level and is smaller than the power supply voltage level.

Claim 4. (currently amended) The source driver of claim 1, wherein the latch further comprises a first level latch and a second level latch, wherein the first level latch sequentially receives digital image data, and

digital image data comprises image data of horizontal lines, and the horizontal lines are sequentially arranged,

when the first latch completely receives image data of one horizontal line, the first latch outputs image data of the one horizontal line to the second level latch, and continues receiving image data of next horizontal line, the second level latch outputs the image data of the one horizontal line to the first level shifter with the positive polarity and the second level shifter with the negative polarity [[the level shifter]].

Claim 5. (currently amended) The source driver of claim 1, wherein the first analog circuit with the positive polarity comprises a digital-to-analog converter with the positive polarity and an output buffer with the positive polarity.

Claim 8. (currently amended) The source driver of claim 1, wherein the second analog circuit with the negative polarity comprises a digital-to-analog converter with the negative polarity and an output buffer with the negative polarity.

2. The following is an examiner's statement of reasons for allowance:

Furuhashi et al. (US 5,731,796) teach a method for driving a liquid crystal display apparatus that includes an LCD panel arranged by a plurality of pixel units formed in a matrix shape, and a signal drive circuit for generating an LCD apply voltage and constructed of at least two integrated circuits.

Wang et al. (US 6,552,708) teach a unit gain buffer of a driver circuit to drive the data line in the filed of LCD data driver.

Yamamoto et al. (US 6,552,708 B1) teach the amplitude expansion circuit as a main part of a drive circuit which includes a VM DC power supply line to which a voltage VM is applied; a VH DC power supply to which a voltage VH roughly twice as high as the voltage VM is applied.

None of the prior art teaches an analog circuit with positive polarity coupled to a power supply voltage level and a first middle voltage level, and an analog circuit with negative polarity coupled to a ground level and a second middle voltage level.

Therefore, the claims are in condition for allowance.

Conclusion

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yong Sim whose telephone number is (571) 270-1189.

The examiner can normally be reached on Monday - Friday (Alternate Fridays off) 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YHS
7/21/07

AMR A. AWAD
SUPERVISORY PATENT EXAMINER